



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Hieu Van TRAN et al.

Serial No.: 09/929,542

Group Art Unit: 2824

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Examiner: Dinh, Son T.

Title: **ARRAY ARCHITECTURE AND OPERATING METHODS FOR DIGITAL MULTILEVEL NONVOLATILE MEMORY INTEGRATED CIRCUIT SYSTEM**

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Rosa A. Caviedes

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AMENDMENT

Box RCE
Commissioner for Patents
Washington, DC. 20231

Sir:

In response to the Office Action mailed on August 27, 2002, please cancel claim 83 without prejudice, and please amend claim 4 as follows: (marked up version of claim in Appendix)

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4. (twice amended) A data storage system comprising:

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a plurality of multidimensional segmented memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, wherein each memory cell is configurable to store one of 2^N values where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells; and